Influence of fabrication steps on optical and electrical properties of InN thin films

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Abstract

This paper reports on a case study of the impact of fabrication steps on InN material properties. We discuss the influence of annealing time and sequence of device processing steps. Photoluminescence (PL), surface morphology and electrical transport (electrical resistivity and low frequency noise) properties have been studied as responses to the adopted fabrication steps. Surface morphology has a strong correlation with annealing times, while sequences of fabrication steps do not appear to be influential. In contrast, the optical and electrical properties demonstrate correlation with both etching and thermal annealing. For all the studied samples PL peaks were in the vicinity of 0.7 eV, but the intensity and full width at half maximum (FWHM) demonstrate a dependence on the technological steps followed. Sheet resistance and electrical resistivity seem to be lower in the case of high defect introduction due to both etching and thermal treatments. The same effect is revealed through 1/f noise level measurements. A reduction of electrical resistivity is connected to an increase in 1/f noise level.

Keywords: indium nitride, low frequency noise and resistivity, morphology, plasma assisted MBE, fabrication

1. Introduction

For the last two decades, nitride semiconductors (AlN, GaN, InN) have been under extensive investigations due to their numerous applications, which span from light-emitting diodes (LEDs) for solid state lighting, to high power and high frequency devices [1–4]. From 2002 onwards, research effort was increased even more, when the optical band gap of InN [5, 6] was re-evaluated to 0.65 eV instead of the earlier 1.89 eV. Therefore, the expected applications of the nitride semiconductors family include multicolour LEDs through the whole spectral range, as well as the highest efficiency heterojunction solar cells. Additionally, with an electron mobility of up to 4000 $cm^2 V^{-1} s^{-1}$ [7] and very high saturation electron velocities ($\sim 4 \times 10^7$ $cm\ s^{-1}$) [3], InN may provide an ideal material platform for electronic transport devices operating up to the terahertz range [8]. To ensure the reliability of commercial devices, an intense fundamental research effort is

required to improve growth mechanisms and processing technology of devices. Among group III nitrides, InN properties, either related to the material or to device application, are poorly known. The presence of an electron accumulation layer at the surface [9], due to strong surface Fermi level pinning (~0.8 eV above the conduction band edge) [4] hinders the fabrication of metal-semiconductor Schottky contacts. The same effect is responsible for the dependence of Hall carrier concentration on InN layer thickness [9, 10]. Despite of this difficulty, InN has already been used in its polycrystalline phase to lower the sheet and electrical contact resistances for different nitride materials (such as InAlN [11], GaN [12, 13]) as well as arsenides [14] and SiC [15], and no degradation was observed over time [14]. Apart from the growth challenge, there lies an additional importance towards the optimization parameters in device processing. The device fabrication processes can influence the material properties as well as the final device performance, as in the case of dielectric passivation [16], plasma and chemical treatments [17, 18], and thermal annealing [19]. In the performance of electronic and optoelectronic devices, high electrical contact and high series resistances reduces the device response speeds. Hence, the optimized device fabrication is essential to obtain an efficient component as an end product. Dry etching is the basic tool used for mesa definition through material removal, and the use of a plasma based treatment induces degradation of the active layer. Thermal processing is known to play a critical role at many stages in device fabrication such as the alloying of ohmic contacts [19], activation of dopant species [20] and implantation induced damage removal [21]. According to literature, InN has not received much attention in terms of processing effects.

Hence, the objective of this work is to study the effect of technological processing steps, in particular the role of the thermal annealing steps (time and sequence) after a plasma based treatment using reactive ion etching (RIE), on optical properties studied by photoluminescence (PL) measurements, surface morphology studied by atomic force microscopy (AFM) and electrical transport behavior (electrical resistivity and low frequency noise) of InN layers. Section 2 describes first the experimental details, such as the characteristics of the In polar InN as-deposited layer, the sample geometries and the fabrication process. Results and discussion are given in section 3 and the main conclusions of our study are summarized in section 4.

2. Experimental details

2.1. In polar InN as-grown layer

The present study involves a series of five 5 mm × 5 mm samples from a 2-inch InN wafer, named A1, A2, A3, A4 and B, respectively. The wafer consisted of a template layer made of a commercial LUMILOG semi-insulating Ga-polar GaN layer (5 μm) grown by metal organic vapour phase epitaxy (MOVPE) on c-plane sapphire substrate. A non-intentionally doped 90 nm thick GaN layer and 400 nm InN layer were

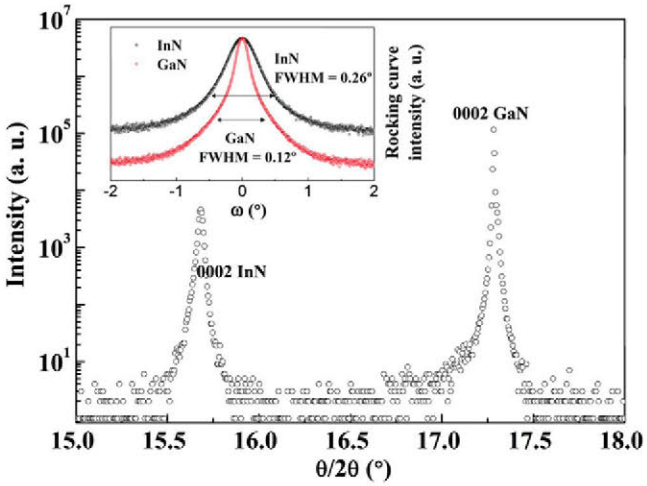

Figure 1. (0002) $\theta/2\theta$ scan of the sample investigated, where InN and GaN peaks show their complete relaxed state, as measured by the angles (15.682° and 17.283°, respectively). The inset depicts the rocking curves of the pseudo-substrate (GaN-on-sapphire) and InN.

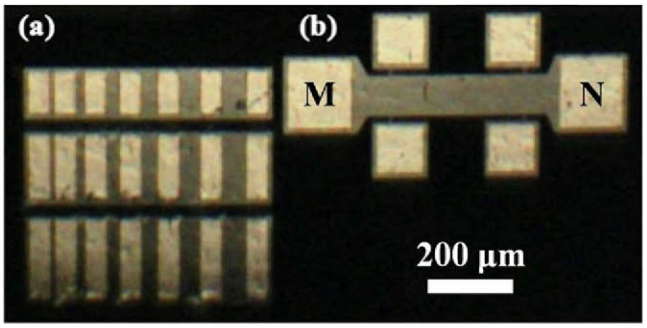

Figure 2. An optical microscope image of one of the samples. (a) Geometry of TLM patterns of three different widths used for sheet resistance and electrical contact resistance measurements and (b) Geometry of the 6 probe pattern used for 4 point contact method with a rectangle length of 300 μm and width of 100 μm, on which electrical resistivity and noise measurements were done.

subsequently grown by plasma assisted molecular beam epitaxy on top of GaN template layer. The In polar InN as-deposited layer was grown under slightly N-rich conditions at a substrate temperature of 400 °C, leading to higher surface electrical concentrations as stated by Fehlberg *et al* [22] compared to the In-rich case. The as-grown InN epilayers were characterized by x-ray diffraction (XRD). Figure 1 exhibits the typical $\theta/2\theta$ XRD profile of the InN film grown on GaN template. The inset shows a comparison of the ω scan XRD rocking curve of 0002 InN with that of GaN. The full width at half maximum (FWHM) is close to values reported in literature [3, 23]. In fact, the good quality material is confirmed by the slight increase in FWHM of InN rocking curve compared to the pseudo-substrate (GaN).

2.2. Sample geometry and fabrication process

2.2.1. Sample geometry. Each sample consists of four patterns repeated all over the 5 mm × 5 mm wafer surface. One of these patterns is shown in the optical microscopic

picture in figure 2. The gold colored regions are metal pads, the dark yellowish ones correspond to InN, and the rest of the dark colored region is GaN after InN etching. Two different geometries were used here. Transmission line method (TLM) geometry shown in figure 2(a), was used to extract the electrical contact and sheet resistances (R_c and R_{sheet}, respectively). Four probe geometry, shown in figure 2(b), was used for low frequency noise measurements. Three TLM widths (W) of 98, 150 and 190 μm were considered. The size of the metallic contact pads is $(W \times 50)\,\mu m^2$. For each TLM width, the distances between contact pads (DCPs) were 56, 48, 38, 30, 19, and 10 μm, respectively. As shown in figure 2(b), the four probe geometry consists of six contact pads among which four were used in measurements: two contact pads across the length are used to apply bias current (M and N in the image), and the other two along either of sides of the rectangle were used to measure the voltage of the device under test. The size of the current and voltage contact pads were $160\,\mu m \times 160\,\mu m$ and $110\,\mu m \times 110\,\mu m$, respectively.

2.2.2. Fabrication process. The fabrication process consisted of two steps: (1) electrical isolation of every device through a mesa (defining of pattern through UV photolithography and dry etching of InN through RIE); (2) fabrication of the metallic contact pads and subsequent thermal annealing (UV photolithography and deposition of the multilayer metal scheme Ti/Al/Ni/Au (20 nm/40 nm/20 nm/80 nm)). The Ti/Al/Ni/Au scheme is fairly standard for n-GaN giving very low electrical contact resistance and high temperature stability [24, 25]. This is the reason why it was chosen for the ohmic contact on InN layer. The RIE was performed using $SiCl_4$:Ar gases (proportion 20:1), with RF power of 125 W to induce plasma formation. The dc bias measured was approximately 390 V, stable during the whole process. As previously shown [26], the use of a combination of chlorine-based and noble gases (such as $SiCl_4$:Ar) increase the selectivity of InN etching over GaN.

Usually, mesa etching induces damage to the material, which can be reduced by thermal annealing. The thermal annealing was done at 400 °C in a nitrogen atmosphere. This particular temperature was chosen, as it is an upper limit for InN to avoid material decomposition [27]. Moreover, Khanna *et al* [28] observed that 400 °C was the annealing temperature at which the lowest sheet and electrical contact resistances could be obtained with Ti/Al/Ni/Au contacts, even though it showed an increase of metal roughness after thermal treatments that could worsen electrical behavior. In order to study the impact of thermal annealing before or after the mesa fabrication, we followed the two fabrication step orders, as shown in the flow chart in figure 3.The fabrication of samples A1, A2, A3 and A4 started with the mesa definition, followed by the deposition of the metallic contact pads and thermal annealing (Process A). For sample B, the metal stack was deposited first, and then it was thermally annealed using the same conditions as before. Mesa definition was performed afterwards (Process B). For samples A1, A2, A3, and A4, annealing time was varied as 0, 5, 10, and 20 min, respectively, whereas for sample B, annealing time was 10 min. In all the cases the samples were cleaned with organic solutions (acetone and isopropanol) after RIE, so that any contamination of the photoresist or from the gases (such as chlorine [29]) can be considered as negligible.

3. Results and discussion

3.1. PL characteristics

Low temperature PL measurements were performed on samples A1, A3 and B to estimate the effects of processing on optical transitions. The two samples (A3 and B), were prior and post thermal annealed for the same amount of time (i.e. 10 min). It is to be noted that A1 is used as the reference sample for both processes. These PL measurements were conducted at 12 K using 488 nm excitation wavelength of an Argon laser. The detection was done with a monochromator and photomultiplier. The InN PL peaks were observed at the vicinity of 0.7 eV (figure 4). The shift in peak energy could be ascribable both to the possible inhomogeneity in sample wafer or to the defect introduction induced by processing effects. We observed a slight variation in PL intensity between process A (samples A1 and A3) and process B (B). No substantial difference between the A1 and A3 is noticed in terms of FWHM, whereas sample B shows a significant increase (see table 1 for the extracted values). This fact suggests a degradation induced by both thermal annealing at a temperature close to the growth temperature and to non-cured plasma (RIE) treatments, leading to formation of non-radiative defects.

3.2. Surface morphology

The results obtained from PL hints towards a degradation mechanism possibly related to surface effects. Increase in roughness could be a reason. Figure 5 shows the $10\,\mu m \times 10\,\mu m$ AFM images of patterned InN samples, and the root mean square (rms) roughness for all the samples is given in table 2. As can be seen, the morphology of all the specimens exhibits platelets propagating in a zigzag manner and surrounded by deep trenches. As annealing time increased up to 10 min, rms roughness of InN mesa surfaces increased from 13.2 nm up to 16.8 nm and thereafter showed a decrement in roughness. The roughness of the metal pads also increased with the annealing time possibly due to the diffusion of metal in the semiconductor and material intermixing. For the same annealing time, the samples A3 and B exhibited similar surface roughness irrespective of technological steps, which means that there is a dependence of surface morphology only on annealing time. Due to that, the observed differences in PL cannot be assigned only to the surface roughness effects. Unexpectedly, a reduction of rms roughness is observed in sample A4, a behavior which is not completely clear, possibly related to a re-accommodation of the crystal structure.

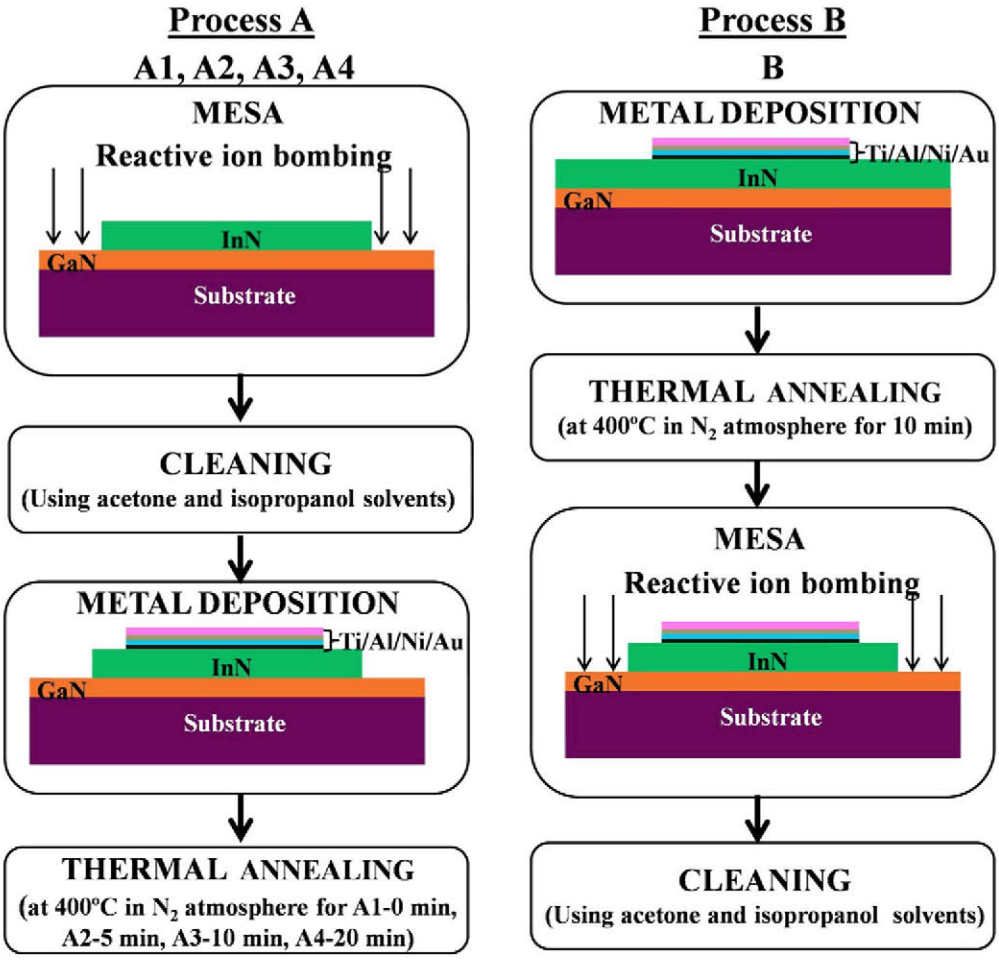

Figure 3. Fabrication steps flowchart for samples (a) A1, A2, A3, A4 and (b) B.

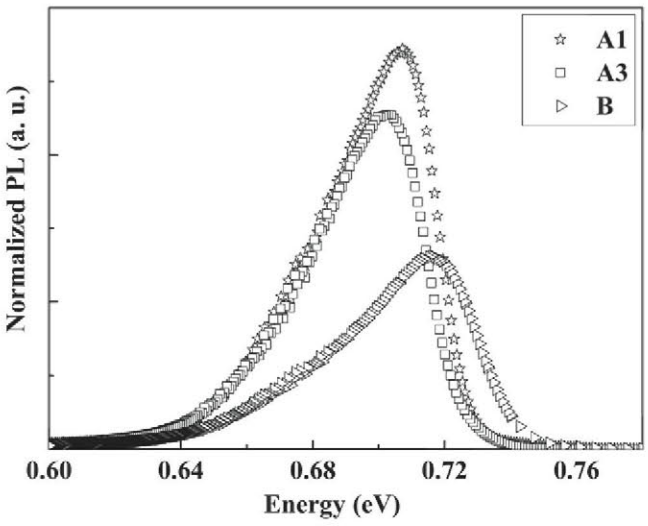

Figure 4. PL spectra on patterned InN layers (samples A1, A3 and B) at 12 K using 488 nm excitation wavelength.

3.3. Electrical properties study at room temperature

Current–voltage (*I–V*) characteristics of all InN samples were measured using a HP 4156B semiconductor parameter analyzer at room temperature. The TLM patterns allow us to extract both the electrical contact resistance (R_c) between metallic pads and InN layer, and the InN sheet resistance (R_{sheet}), also named as resistance per square, is equal to the ratio of the electrical resistivity over the InN film thickness. An example of *I–V* measurements performed on A1, across 190 μm wide TLM pattern for all the available spacing between the metallic pads (DCP), is shown in figure 6(a). Figure 6(b) presents the corresponding measured electrical resistance as a function of DCP for the three TLM widths of A1. The data were fitted using a linear regression, and the intercept of linear fitted curves at *y* axis is equal to $2R_c$ and the slope gives R_{sheet}/W [30].

The measured R_c was always 100 to 1000 times smaller than the measured InN electrical resistance. The highest R_c value was approximately 0.5 Ω while in some cases it was of the same order of the system resolution. R_c is weakly sensitive to the difference in technological step order while it is strongly dependent on the metal/semiconductor contact. For each sample, the measured sheet resistance was quite similar for three different TLM widths, which confirmed good

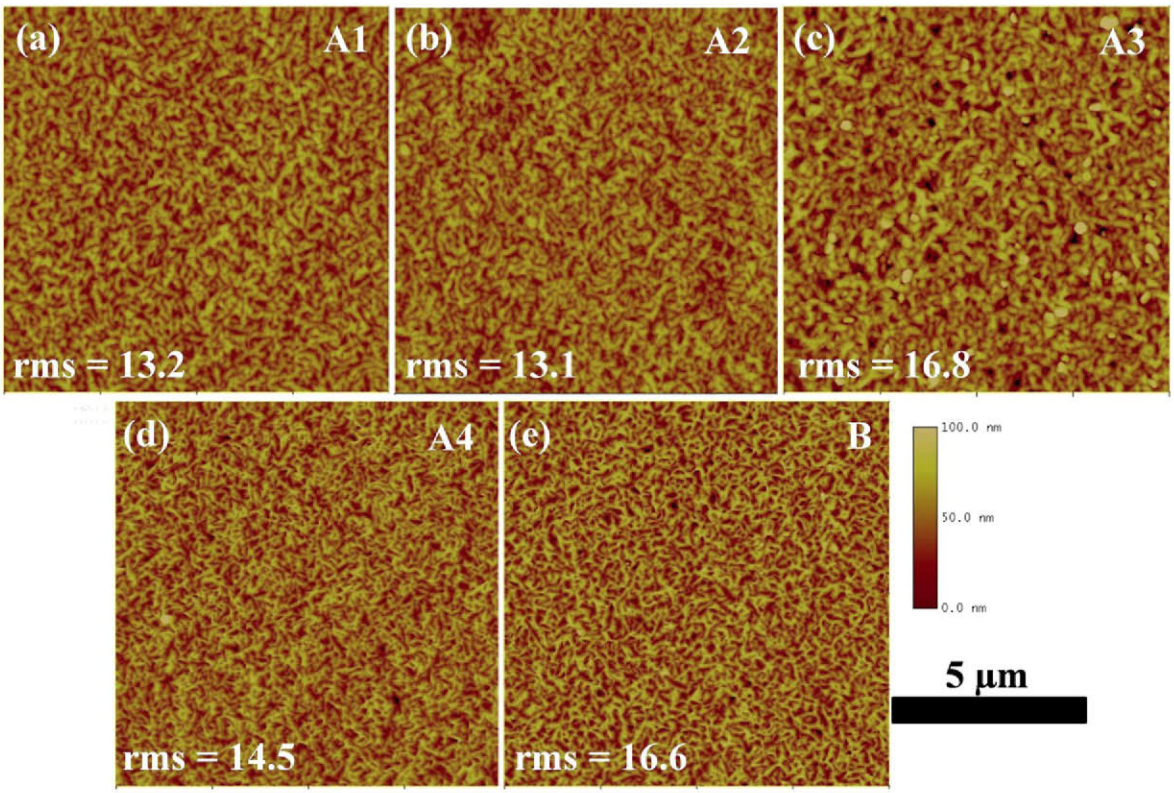

Figure 5. AFM images of InN samples (a) A1 (non annealed sample) (b) A2 (annealing time = 5 min). (c) A3 (annealing time = 10 min), (d) A4 (annealing time = 20 min) and (e) B (annealing time = 10 min).

Table 1. Values extracted from PL measurements for the samples investigated. Note that the intensity of the peaks is rescaled to the intensity of the reference sample (A1).

Sample	Process type	Annealing time (min)	PL peak energy (eV)	PL intensity (a.u.)	FWHM (meV)
A1	Reference	0	0.707	1	39.8
A3	A	10	0.703	0.83	40.6
B	B	10	0.717	0.43	46.1

Table 2. The measured surface roughness of InN surface and metal pads.

			rms roughness (nm)	
Sample	Process type	Annealing time (min)	InN surface	Metal pad
A1	A	0	13.2	13.4
A2	A	5	13.1	20.8
A3	A	10	16.8	26.2
A4	A	20	14.5	23.0
B	B	10	16.6	26.9

surface homogeneity of InN wafer. R_{sheet} increased with annealing time up to 10 min and then decreased (as shown in figure 7).

This result suggests that a defect generated after etching treatments can create donor-type defects reducing the total sheet resistance. The thermal annealing can cure this effect by increasing the total sheet resistance for annealing time up to 10 min (A2 and A3). Increasing the annealing time could probably induce more defects, either at surface or in the bulk, and reducing again the sheet resistance (A4). The lowest sheet resistance was observed for sample B, for which metallization was performed prior to electrical isolation. In this case both plasma and thermal treatments are causes for increasing defects. This fact can have an empirical justification taking into account the expression for R_{sheet}:

$$R_{sheet} = \frac{1}{n \times e \times \mu} \tag{1}$$

Where n is charge carrier density (electrons), e is the charge of electron and μ is the carrier mobility. As previously stated, the processing treatments, such as mesa etching, will increase the density of defects. An increase in defect density will cause a drop in mobility and hence an increase both in electrical resistivity and R_{sheet}. Therefore, in this case to account for a drop in R_{sheet} we have to assume an increase in the electron density. However, R_c only depends on the nature of the metal/semiconductor interface, R_{sheet} can be correlated with material modifications during processing.

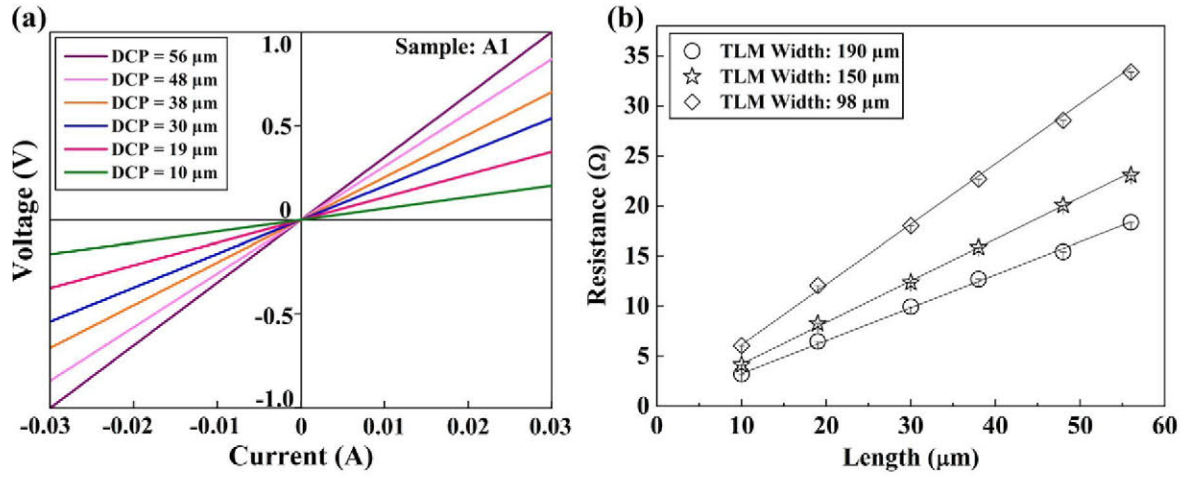

Figure 6. (a) Example of *I–V* measurements performed on sample A1 at 300 K using the 190 μm wide TLM for all the available DCPs, and (b) measured electrical resistance as a function of DCP for sample A1 and for the three TLM widths.

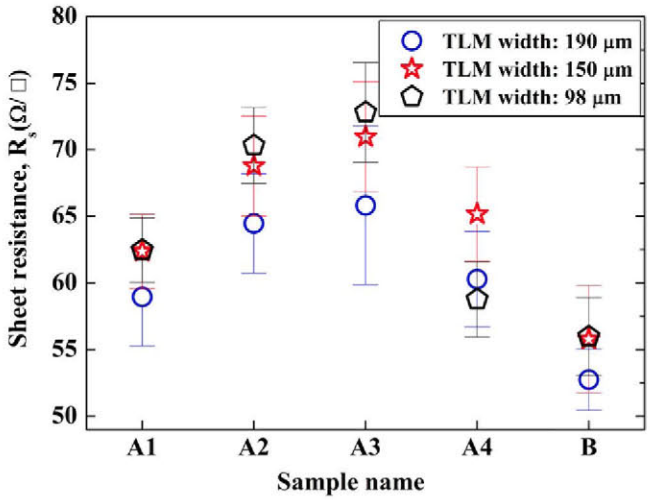

Figure 7. Sheet resistances of the samples investigated using three different TLM structures at 300 K.

A more detailed study of electrical transport properties was made using the four probe technique on the geometry shown in figure 2(b) by measuring electrical resistivities (ρ) and 1/f noise levels. It is to be noted that electrical resistivities are calculated by taking into account the nominal thickness of the InN layers, and they are in agreement with the R_{sheet} values. For all the studied samples, the results are in agreement with literature [31]. The low-frequency voltage–noise analysis was performed at 300 K with a homemade low noise electronics read out associated with a HP 3562A dynamic signal analyzer at various bias currents [32]. The spectra were acquired in the 10 Hz to 100 kHz frequency range. A typical frequency dependence of spectral density (S_v) of voltage fluctuation processes in the investigated thin films is shown for A3 in figure 8(a). Apart from a number of peaks at definite frequencies due to external noise sources, all the spectral density traces are seen with two main components. The first component shows $1/f$ dependence at low frequencies. The other one shows a constant amplitude spectrum, corresponding to white noise mainly due to the instrument background noise (equal to 2.8×10^{-17} V^2 Hz^{-1}) and thermal noise (equal to $4k_BTR$), where k_B is Boltzmann constant, T is temperature, and R is measured electrical resistance. The low frequency noise voltage spectral density S_v has a quadratic dependence with the bias current. This 1/f noise level at 1 Hz and at a voltage across the measured device of 1 V is defined as K_v (which is a dimensionless parameter). This gives a measurement of InN layers' electrical quality and is plotted for all samples in figure 8(b). We observed a slight change of K_v values depending on processing steps. Thermal anneal seems to reduce the noise, even if the annealing time was short, the low frequency noise level reaches a constant value $\sim 2 \times 10^{-14}$. In the case of sample B, noise measurements confirm the fact that both plasma etching and thermal annealing at a temperature close to growth/decomposition temperature is likely to induce defects increasing noise levels and noise dispersion among test structures. It has to be noted that the noise levels obtained here are among the lowest ever reported on InN [33].

The Hooge parameter (α_H) was calculated by using the Hooge semi-empirical relation [34] which is given by

$$K_v = \frac{\alpha_H}{n \times L \times W \times t} \tag{2}$$

where, n is charge carrier density (cm^{-3}), $(L \times W \times t)$ is sample volume (cm^3). Taking the sample dimensions as $W = 305\,\mu$m, $L = 100\,\mu$m and $t = 400$ nm and assuming a constant charge carrier concentration in between 10^{18}–10^{20} cm^{-3} from literature [3, 35, 36], we obtained α_H of about 10^{-4}–10^{-6}. In the estimation of the electron concentration we considered two extremes, correspondent to bulk concentration (10^{18} cm^{-3}) [3, 35] and surface electron concentration (10^{20} cm^{-3}) [36]. The lowest value obtained can be compared favorably with other narrow band gap semiconductors, such as InAs for which it is about 10^{-3} at room temperature [37].

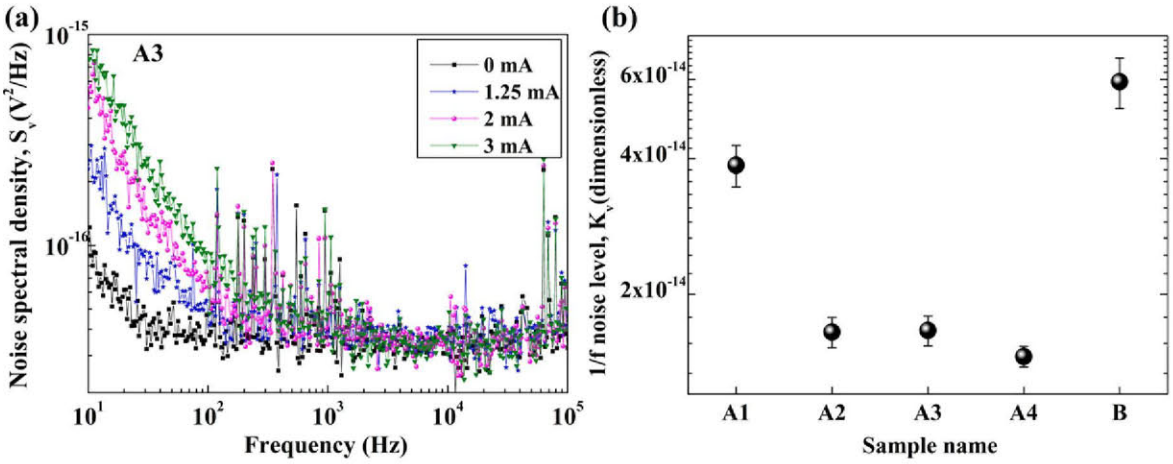

Figure 8. (a) Voltage noise spectral density for different dc bias currents for sample A3 at 300 K and (b) 1/f noise levels of all 5 samples (A1, A2, A3, A4 and B).

4. Summary

A case study has been done in understanding the influence of processing steps on the properties of InN electrical contacts and material. The investigation was conducted on a set of samples from the same wafer subjected to a different order of processing steps (etching and metallization) and thermal treatments. PL characterization gave a correlation of processing steps and optical degradation of the material. In particular an annealing of 10 min at 400 °C after the device fabrication (RIE and metallization) did not substantially change the optical emission, while the same thermal annealing before the InN etching caused a slight quenching in PL intensity as well as an increase in FWHM. The dependence of the rms roughness on annealing time and not on the technological steps suggests discarding the origin of this observed effect only on surface modifications. While it is believed that electrical contact resistance depends only on metal/semiconductor interface, the measurement of sheet resistance makes us think of a mechanism related to surface and bulk induced defects. The effect observed suggests that annealing time up to 10 min reduces the defect-assisted conduction mechanism, while an increase in time will likely introduce more conductive paths. Annealing before the etching treatment (not cured) induces, in fact, more conduction leading to the lowest sheet resistance. Low frequency noise measurements instead, gave a clear trend of the processing effects: assuming that defects induce a higher noise (K_v), thermal annealing after mesa recover damages possibly induced by etching, reducing in this way 1/f noise levels. This recovery is obtained after 5 min, the low frequency noise is then constant even if the annealing time is increased. A double competing mechanism could be in fact involved: a reduction in noise due to annealing and degradation of the electrical properties due to annealing at a temperature close to the growth and dissociation temperature. In fact, when the annealing is performed before RIE (sample B), both effects sum up giving higher noise levels with a higher dispersion among devices, lower PL intensity and higher FWHM, lower R_{sheet} and higher surface rms roughness. Both surface and bulk properties are likely to be affected. All these facts can suggest increased carrier concentration due to defect introduction and properties degradation in sample B. For the best optimization in terms of material and electrical properties, process A is more appropriate. In particular, a thermal anneal of 10 min at 400 °C is likely to give highest sheet resistance, due to reduction of defects contributing to conduction, and low noise levels.

Acknowledgements

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